Microprocessors and Micro-controllers

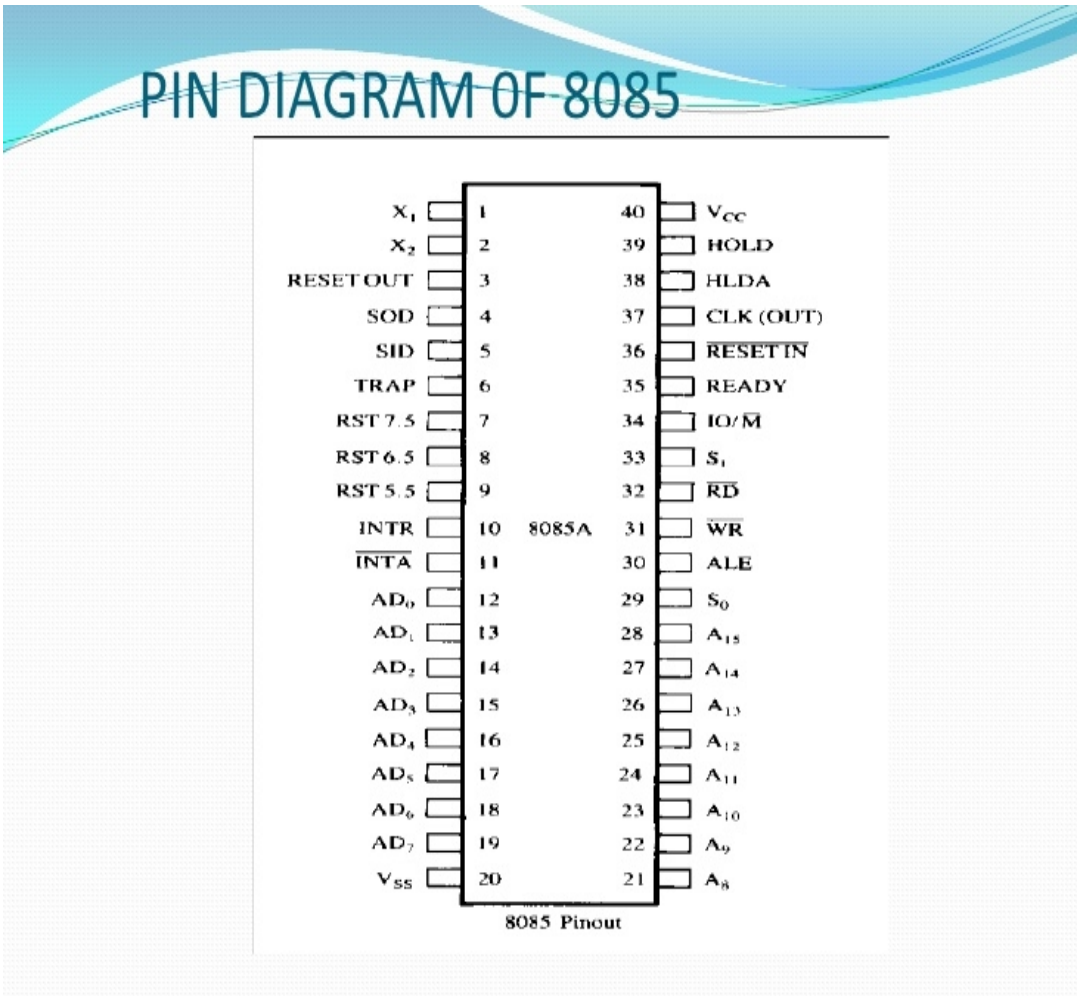
Class 4

8085 Pin description.

The Intel 8085 is a complete 8 bit parallel central processing unit (CPU), having a total of 40 pins. The 8085 uses a multiplexed data bus. The address is split between the 8bit address bus and the 8bit data bus.

8085 microprocessors have the following Properties:

- Single + 5V Supply
- 4 Vectored Interrupts (One is Non Maskable)
- Serial In/Serial Out Port
- Decimal, Binary, and Double Precision Arithmetic
- Direct Addressing Capability to 64K bytes of memory



8085 Pinout

The different sections of the pins can be categorized into 5 types as per their activities:

1. Memory and IO Control unit - 23 lines (16 pins for data/address and 7 pins for control)
2. CPU and Bus Control unit - 10 lines
3. Timing Control unit - 3 lines
4. Serial data transfer - 2 lines
5. Power supply unit - 2 lines

1. Memory and IO control lines

Address and Data lines (AD_0 - AD_7) : has 8 pins (pin no. 12 to 19)
Address lines (A_8 - A_{15}) : has 8 pins (pin no. 21 to 28)

- There are 8 Address-Data bits (bi-directional), connected to the 8-bit data bus for input and output of data to and from Memory/IO devices to the CPU.
- There are 8 address bits (uni-directional), which works along with the 8 data bits, to form a total of 16 bits, which are connected to the 16-bit address bus for sending the address from CPU to the memory/IO devices.
- The address-data bits (AD_0 - AD_7) are used to send and receive data and only to send addresses from Memory/ IO ports, and this is done through Time-division multiplexing, i.e. Lower 8 bits of the memory address (or I/0 address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles.
- The higher bits of the 16-bit address appears in the Address bus, in the first clock cycle only to form the 16-bit address in the Address bus.

ALE - Address Latch Enable (pin no 30)

- This is enabled in the first clock pulse, so that the address-data bits (AD_0 - AD_7) are multiplexed to carry address at this time. Then it gets disabled, so that the same bits can carry 8-bit data in the data bus.

IO/M (Output) (pin no 34)

- IO/M indicates whether the Read/Write is to memory or I/O port.

S_0 and S_1 - The Status Lines (pin no 29 and 33 respectively)

- This tells in what state the micro-processor is working. The following values and states are available, as given in the table below:

S_1	S_0	States
0	0	HALT
0	1	READ
1	0	WRITE
1	1	FETCH

RD - The Read pin (pin no 32)

- This indicates that the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer.

WR - The Write pin (pin no 31)

- This indicates that the data on the Data Bus is to be written into the selected memory or I/O location.

READY (Input) (pin no 35)

- READY is used for slow I/O or memory interfacing with CPU.
- If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

2. CPU and Bus Control lines

HOLD - Input line (pin no 39)

- This indicates that DMA (Direct Memory Access) is requesting the use of the Address and data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue and the processor can regain the buses only after the Hold is removed.

HLDA - Output line (pin no 38)

- HOLD ACKNOWLEDGE indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

TRAP (input), RST 7.5, RST 6.5, RST 5.5 (pin no 6, 7, 8, 9 respectively)

- Trap interrupt is a non-maskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.
- RESTART INTERRUPTS; These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.
- RST 7.5 has the Highest Priority and RST 5.5 has the Lowest Priority
- These interrupts have a higher priority than the INTR.

INTR (Input) (pin no 10)

- INTERRUPT REQUEST is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction.
- If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued.
- During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine.
- The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

INTA (Output) (pin no 11)

- INTERRUPT ACKNOWLEDGE is used instead of (and has the same timing as) RD during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.

RESET IN (Input) (pin no 36)

- Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flipflops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output) (pin no 3)

- Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

3. Timing and Control Unit

X_1, X_2 (Input) (pin no 1 and 2 respectively)

- Crystal or R/C network connections is supplied from outside to set the internal clock generator. X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.
- The Crystal Quartz is connected with the X1 and X2 pins of the processor.

CLK (Output) (pin no 37)

- Clock Output is used as a system clock when a crystal or R/ C network is used as an input to the CPU. The period of CLK is twice the X1, X2 input period.

4. Serial data transfer I/O lines

SID (Input) (pin no 5)

- This is the Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
- In 8085 Instruction set, RIM stands for “Read Interrupt Mask”. It is a 1-Byte multi-purpose instruction. It is used for the following purposes.
    1. To check whether RST7.5, RST6.5, and RST5.5 are masked or not
    2. To check whether interrupts are enabled or not
    3. To check whether RST7.5, RST6.5, or RST5.5 interrupts are pending or not
    4. To perform serial input of data.

SOD (output) (pin no 4)

- Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
- In 8085 Instruction set, SIM stands for “Set Interrupt Mask”. It is 1-Byte instruction and it is a multi-purpose instruction. The main uses of SIM instruction are –
    1. Masking/unmasking of RST7.5, RST6.5, and RST5.5
    2. Reset RST7.5 flip-flop to 0
    3. Perform serial output of data

5. Power supply lines

Vcc (pin no 40) : +5 volt supply.

Vss (pin no 20) : Ground Reference

8085/8085A Functional Description

- The 8085A is a complete 8 bit parallel central processor. It requires a single +5 volt supply. Its basic clock speed is 3 MHz. Also it is designed to fit into a minimum system of three IC's: The CPU, a RAM/ IO, and a ROM or PROM/IO chip.

- The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower 8 bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or l/O data.

- The 8085A provides RD, WR, and lO/Memory signals for bus control. An Interrupt Acknowledge signal (INTA) is also provided. Hold, Ready, and all Interrupts are synchronized. The 8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

- In addition to these features, the 8085A has three maskable, restart interrupts and one non-maskable trap interrupt. The 8085A provides RD, WR and IO/M signals for Bus control.

Status Information

- Status information is directly available from the 8085A. ALE serves as a status strobe. The status is partially encoded, and provides the user with advanced timing of the type of bus transfer being done. IO/M cycle status signal is provided directly also. Decoded S_0, S_1 Carries the following status information HALT, WRITE, READ, FETCH.

- S_1 can be interpreted as R/W in all bus transfers. In the 8085A the 8 LSB of address are multiplexed with the data instead of status.

Interrupt and Serial l/O

- The8085A has 5 interrupt inputs: INTR, RST5.5, RST6.5, RST 7.5, and TRAP. Each of the three RESTART inputs, 5.5, 6.5. 7.5, has a programmable mask. TRAP is also a RESTART interrupt except it is non- maskable.

- The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

- The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP highest priority, RST 7.5, RST 6.5, RST 5.5, INTR lowest priority.

- 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine. The TRAP interrupt is useful for catastrophic errors such as power failure or bus

error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive.

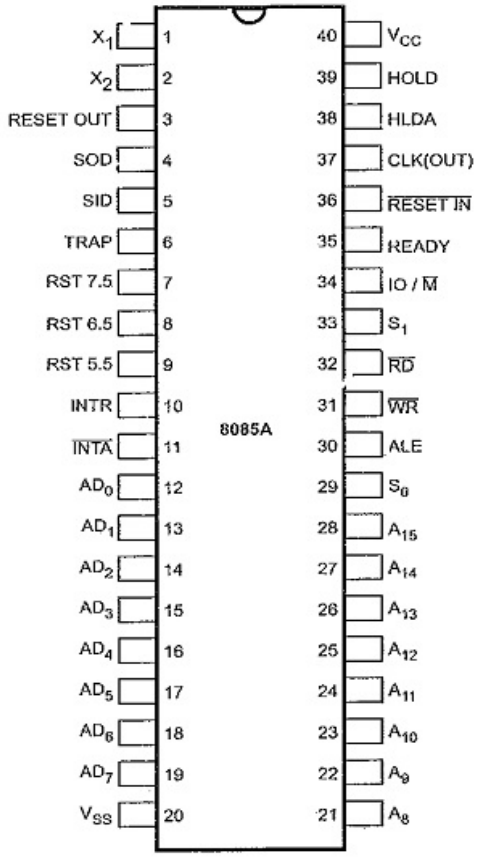


Fig. 1.3 (a) Pin configuration

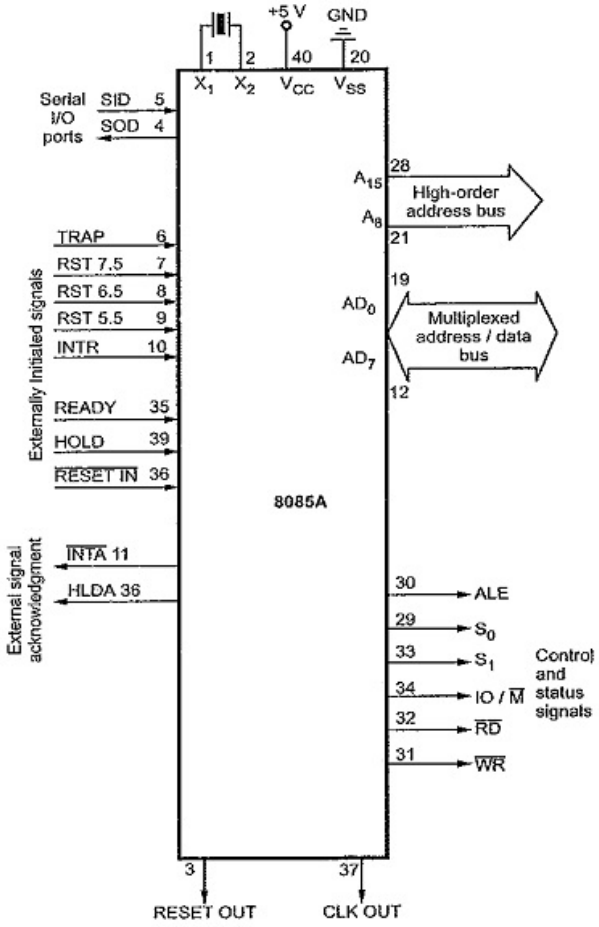


Fig. 1.3 (b) Functional pin diagram